Solution-Processed Nanocrystalline TiO$_2$ Buffer Layer Used for Improving the Performance of Organic Photovoltaics

Teddy Salim, Zongyou Yin, Shuangyong Sun, Xiao Huang, Hua Zhang,* and Yeng Ming Lam*

School of Materials Science and Engineering, Nanyang Technological University, 50 Nanyang Avenue, Singapore 639798, Singapore

Ⓢ *Supporting Information*

ABSTRACT: In this study, we use solution-processable crystalline TiO$_2$ nanoparticles as a buffer layer between the active layer and aluminum cathode to fabricate the P3HT:PCBM-based bulk heterojunction (BHJ) organic photovoltaic (OPV) devices. The employment of the presynthesized TiO$_2$ nanoparticles simplifies the fabrication of OPV devices because of the elimination of an additional hydrolysis step of precursors in air. The fabricated OPV devices with the thermally stable TiO$_2$ buffer layer are subjected to the further postdeposition thermal annealing, resulting in a power conversion efficiency (PCE) as high as 3.94%. The improved device performance could be attributed to the electron transporting and hole blocking capabilities due to the introduced TiO$_2$ buffer layer.

KEYWORDS: buffer layer, TiO$_2$, nanoparticles, bulk heterojunction, photovoltaics, polythiophene
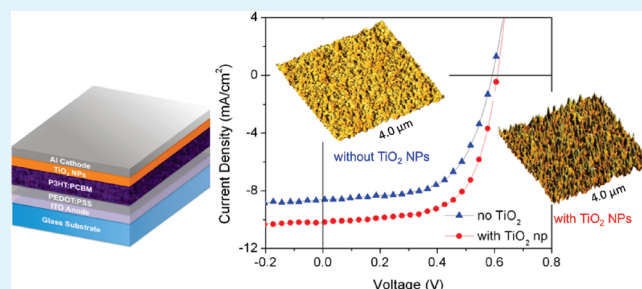
■ INTRODUCTION

As one of the promising renewable energy resources, polymer-based organic photovoltaics (OPVs) have attracted significant interest in scientific and industrial communities in the past decade because of their potential for the realization of low-cost, printable, lightweight, large-area and flexible devices.[1−4] A typical OPV device architecture consists of nanocomposites of both electron-donating (*p*-type) polymers and electron-accepting (*n*-type) fullerenes, commonly termed as bulk heterojunction (BHJ), sandwiched between two electrodes with different work functions. Recent works on BHJ-based OPVs have showed much progress in the improvement of OPV performance, e.g. the high power conversion efficiency (PCE), 5−7%, was achieved.[5−8] One of the main strategies employed to enhance the PCE is to engineer the electrode interface by sandwiching a buffer layer between the active layer and the electrodes.[9] A variety of materials have been deposited through vacuum evaporation or solution processes as the buffer layer, such as metals (Ca, Ba),[10,11] salts (LiF, Cs$_2$CO$_3$),[12] transition metal oxides (oxides of Cr, Zn, Ni),[13−16] and organic materials.[17,18]

TiO$_2$ synthesized by established synthetic routes[19,20] is commonly used for photovoltaics as *n*-type materials.[21,22] Recently, solution-processed titanium suboxide (TiO$_X$) has been applied in both single and tandem OPV devices as a multifunctional buffer layer serving as the optical spacer, electron transport/hole blocking layer (ETL/HBL) and oxygen barrier.[23−33] The preparation of TiO$_X$ involves the sol−gel synthesis of precursors, followed by spin-coating and exposure of TiO$_X$ precursor layer to the ambient atmosphere, which complicates the device fabrication and risks the degradation of OPV active materials. In addition, the TiO$_X$ layer is less stable when subjected to the

high-temperature treatment, thereby limiting exclusively to thermal annealing before cathode deposition.[34] Therefore, a simple coating process of thermally stable TiO$_2$ without the requirement of the additional hydrolysis of precursors in the air is deemed necessary.[35,36]

In this study, we introduce an OPV buffer layer prepared from the solution-processed nanocrystalline TiO$_2$ nanoparticles. Our approach is to first convert the precursors into oxides before coating the oxide solution onto the active layers. Introduction of this solution processable, thermally stable TiO$_2$ buffer layer improved the PCE of devices to 3.94%, ca. 27.5% higher those without TiO$_2$ buffer layer.

■ EXPERIMENTAL SECTION

The synthesis of TiO$_2$ nanoparticles was performed as follows. TiO$_2$ sol (33 mM) was prepared from the hydrolysis of titanium-tetraisopropoxide (Ti(OCH(CH$_3$)$_2$)$_4$) precursor (Aldrich). After 0.4 mL of 0.2 M HCl was diluted in 18 mL of ethanol, 0.2 mL of the precursor (99.9%), initially dissolved in 1.9 mL of ethanol, was added dropwise into the vigorously stirred HCl at 0 °C. The mixed solution was then stirred for 5 h to give a transparent TiO$_2$ sol, followed by ten-time dilution in ethanol. The sol was further heated in an autoclave at 160 °C for 16 h to form crystalline TiO$_2$ nanoparticles (TiO$_2$ NPs). TEM images of the synthesized TiO$_2$ nanoparticles were obtained with JEOL JEM 2010F operated at a working voltage of 200 kV. XRD was performed using X-ray diffractometer Siemens D-500 (Bruker AXS, Inc.). The OPV structure with a buffer layer of TiO$_2$ NPs is shown in Figure 1a. The device was fabricated using the following steps. After the ITO-coated
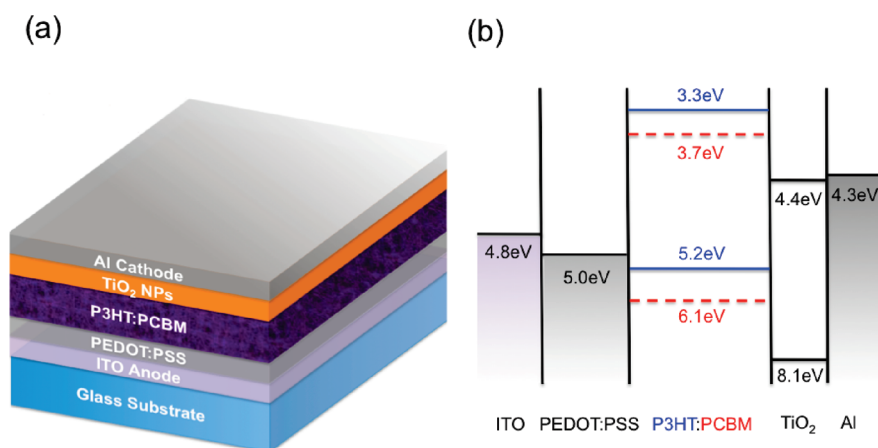
Figure 1. (a) Schematic illustration of the fabricated OPV device. (b) Energy level diagram in the OPV device.
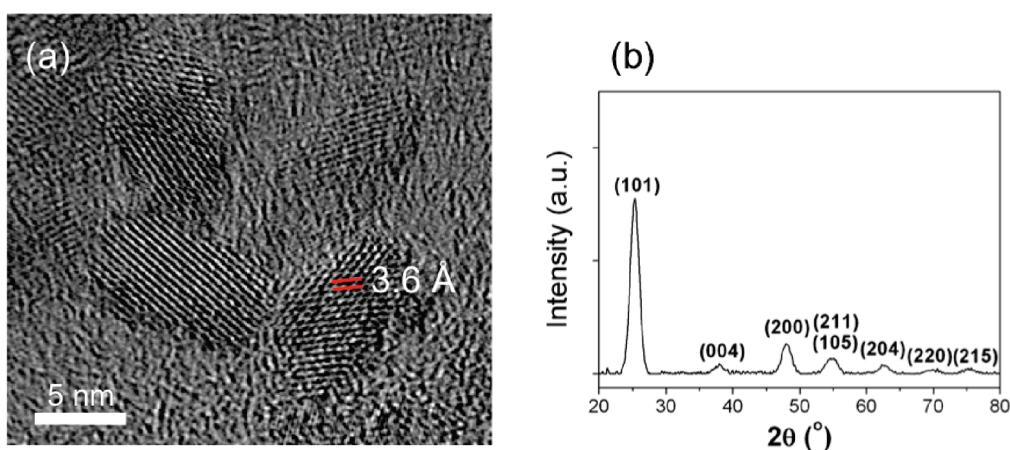

Figure 2. (a) HRTEM image and (b) XRD pattern of the synthesized TiO_2 nanoparticles.

glass substrates were sequentially cleaned by ultrasonication in DI water, acetone and isopropyl alcohol, they were plasma-cleaned for 2 min using Harrick PDC-32G plasma cleaner. Then a ca. 30 nm thin layer of PEDOT:PSS (H. C. Stark, CLEVIOS) was spin-coated onto the cleaned ITO substrates, followed by baking on a hot plate at 140 °C for 10 min. After transferring the substrates into the N_2 glovebox, the blend solution of poly(3-hexylthiophene) (P3HT, Rieke Metals):[6,6]-phenyl-C61-butyric acid methyl esther (PCBM, Nano-C) (10:8 wt %, 18 mg/mL in o-DCB) was spin-coated onto the PEDOT:PSS on ITO at 700 rpm for 2 min, resulting in an active layer of 95 ± 5 nm. After the TiO_2 NP solution was spin-coated on P3HT:PCBM at different rates (1000 - 4000 rpm) for 60 s in the glovebox (with H_2O of ca. 1 ppm), the Al electrode (ca. 100 nm) was thermally evaporated at low pressure (<1 × 10^{-6} Torr). The device with an active area of 0.07 cm^2 was obtained. Finally, all the devices were thermally annealed on a hot plate at 150 °C for 20 min. For comparison, devices without TiO_2 buffer layer were also prepared using similar fabrication conditions. Current density–voltage (J–V) curves were measured in ambient atmosphere under simulated AM 1.5G illumination (100 mW/cm^2) using a Keithley SMU 2400 sourcemeter. The incident-photon-to-current (IPCE) measurement was performed using the Merlin radiometer (Newport) with a monochromator-calibrated wavelength control. A calibrated Si photodiode (Hamamatsu) was used as the reference device for the counting of incident photons. AFM images were obtained using Digital Instruments (Veeco), and the data obtained were processed with WSxM 5.0 (Nanotec Electronica).[37]

RESULTS AND DISCUSSION

The energy level diagram in Figure 1b shows that the coated TiO_2 layer fulfills the requirement as both electron transport layer (ETL) and hole blocking layer (HBL). The lowest-unoccupied molecular orbital (LUMO) level of TiO_2 (4.4 eV) matches well with the Fermi level of Al (4.3 eV) and may facilitate the electron transfer from PCBM (LUMO level: 3.7 eV) to Al.[31] On the other hand, the highest-occupied molecular orbital (HOMO) level (8.1 eV) of TiO_2 is larger than that of P3HT (5.2 eV), resulting in the prevention of the hole accumulation at the active layer-cathode (Al) interface, which leads to a more reduced interfacial charge recombination.

Transmission electron microscopy (TEM) was used to characterize the synthesized TiO_2 nanoparticles. As shown in Figure S1 in the Supporting Information, the measured diameter of TiO_2 NPs is 4–9 nm. The high-resolution TEM (HRTEM) image (Figure 2a) shows the TiO_2 is crystalline, in which a lattice spacing of 3.6 Å is assigned to the (101) planes. X-ray diffraction (XRD) was also used to characterize TiO_2 NPs (Figure 2b), which indicates the existence of nanocrystallinity in the sample, and the peaks indicate that the particles are anatase TiO_2 without any impurities.[35,38,39] In contrast, most of the reported TiO_X layers so far are amorphous as indicated by the absence of XRD peaks.[31] Crystalline semiconductors generally have higher carrier
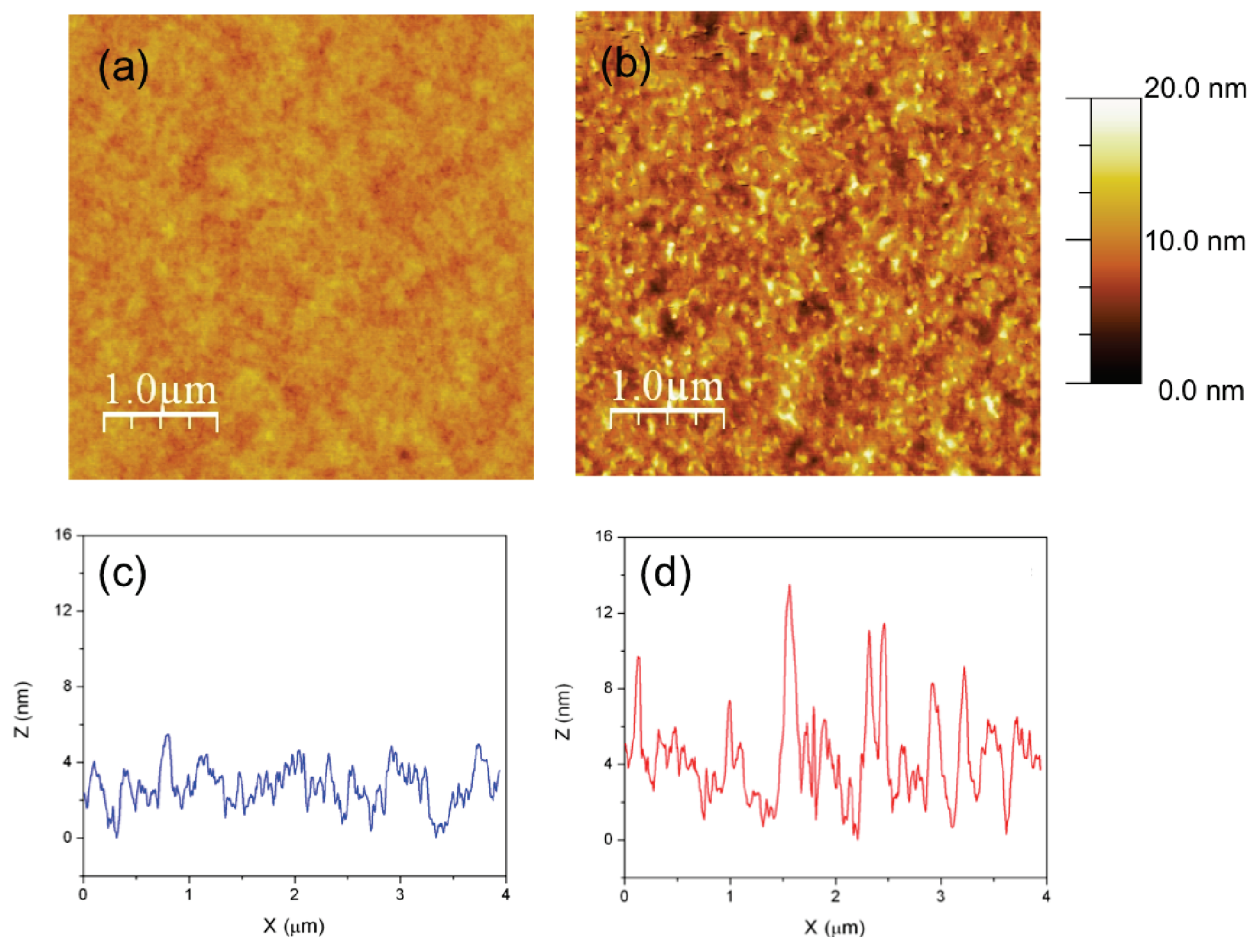
Figure 3. AFM topographic images of (a) P3HT:PCBM and (b) TiO$_2$ buffer layer coated on P3HT:PCBM. Typical line profiles of (c) P3HT:PCBM and (d) TiO$_2$ buffer layer coated on P3HT:PCBM.

mobility than do their amorphous counterparts,[40] suggesting that the electrons in crystalline TiO$_2$ NPs have higher diffusion length, therefore relaxing the constraint imposed on the buffer layer thickness.

Figure 3 shows both AFM topography images and typical line profiles of the blend thin films with and without TiO$_2$ NP coating. Figure 3a shows that the P3HT:PCBM film is smoother, while TiO$_2$ coating results in a rougher surface with many obvious protrusions (Figure 3b), which we believe are TiO$_2$ aggregates with lateral size of about 0.1 μm and height of 4−14 nm. The root-mean-square (rms) surface roughness value of the TiO$_2$-free and TiO$_2$-coated blends is 1 and 2.4 nm for 4 × 4 μm^2, respectively. The characteristic of the TiO$_2$ surface is different from that of TiO$_X$, which has often been reported to be smooth.[23,31] Importantly, the blend of unannealed TiO$_2$ layer shows a similar profile with the postannealed one, suggesting that the thermal treatment has little or no effect on the TiO$_2$ buffer layer. The unchanged morphology suggests higher thermal stability of the TiO$_2$ layer.

Figure 4a shows the typical current density−voltage (J−V) characteristics of devices with and without TiO$_2$ buffer layer under AM 1.5G one-sun illumination. The detailed device parameters are summarized in Table 1, and the statistical distribution of these parameters based on the performance of 10 devices is presented in Figure S2 in the Supporting Information. The OPV device with a *ca.* 100 nm thick blend film, but without TiO$_2$ NP

buffer layer, exhibits power conversion efficiency (PCE) of 3.09%, with short-circuit current (J_{SC}) of 8.62 mA/cm^2, open-circuit voltage (V_{OC}) of 0.59 V and fill factor (FF) of 0.60. These parameters are considered to be relatively high for a ca.100 nm thick blend film without any buffer layer, which could be a result of the morphological optimization induced by the postdeposition annealing treatment. To investigate how the film of nanocrystalline TiO$_2$ NPs affects the device performance, TiO$_2$ sol was spin-coated at various rates (1000−4000 rpm), and the results are summarized in Table 1. Compared to the device without TiO$_2$ layer, the best device we obtained with TiO$_2$ buffer layer gives ca. 27.5% increase of PCE from 3.09 to 3.94%, J_{SC} of 10.18 mA/cm^2, V_{OC} of 0.61 V and FF of 0.64. For the devices with TiO$_2$ buffer layer, the device improvement mainly derives from both J_{SC} and FF, whereas V_{OC} remains almost constant ca. 0.6 V. It is known that V_{OC} can be approximated from the difference between HOMO of *p*-type material and LUMO of *n*-type material.[41] Although the additional TiO$_2$ layer may help to break the symmetry of electric field in the device, its LUMO level, which is close to the Fermi level of Al, does not have much contribution to V_{OC}. On the contrary, increase in V_{OC} upon TiO$_2$ layer insertion has been reported by Park et al.[35] However, it should be noted that in their case, the V_{OC} of the control device without TiO$_2$ is lower, i.e., 0.42 V, which is presumably due to the variation in processing conditions.

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The improvement in both J_{SC} and FF is expected as the TiO_2 buffer layer functions as ETL and HBL, inducing a more efficient charge collection with reduced active layer-cathode interfacial charge recombination. Recently, Lee et al. found that the TiO_X layer in OPV decreases the saturation current density, resulting in reduced minority carrier density.[42] TiO_2 with lower HOMO provides higher energy barrier for holes, and therefore moderating the charge injection process and leading to higher FF.

Besides used as ETL/HBL, the introduction of TiO_2 buffer layer can redistribute the light intensity in the blend film, i.e. as an optical spacer, which hence enhances the photon harvesting. Therefore, it is critical to fine-tune the thickness of both the TiO_2 buffer layer and active layer. In our study, the improved J_{SC} should be less attributed to the role TiO_2 as optical spacer considering the nonuniformity of TiO_2 thickness. Besides, the rough TiO_2 may also aggravate light scattering at the oxide/metal interface.[43] The argument on redundancy of optical spacer has been presented by Andersson et al., who pointed out that the blend film with optimized thickness does not need optical spacer for enhancement of light absorption.[44]
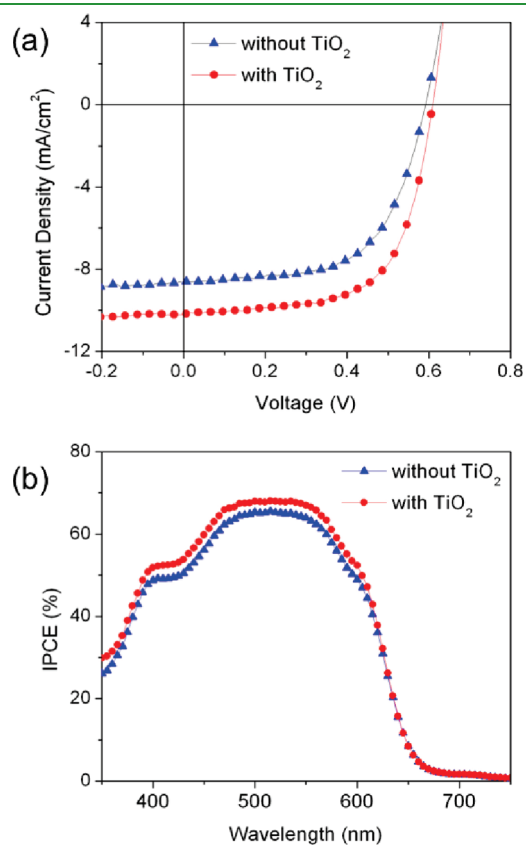
The series resistance (R_s) and shunt resistance (R_{sh}), calculated from the inverse slope of J–V characteristics at V = 0 V and V = V_{OC}, respectively, are shown in Table 1. Incorporation of TiO_2 buffer layer generally lowers R_s by ca. 31.9−42.5%, while increasing R_{sh} by ca. 34.5−54.5%. The reduction in R_s correlates well with the enhancement in J_{SC}.[45,46] The improved R_{sh} suggests that the TiO_2 buffer layer decreases the leakage current of devices since it is used as the protective layer, that prevents the charge escaping from cathode to the active layer, e.g. at the pinhole regions.

Most of the reported devices fabricated with TiO_X layer used for OPV the preannealing technique to optimize their blend morphology. Wang et al. confirmed that the postannealing of the device with unmodified TiO_X layer resulted in severe degradation in device performance, ca. 66% drop in PCE as compared to the device with preannealing.[34] In our study, the opposite effect was observed even under similar annealing conditions, suggesting TiO_2 NPs are thermally more stable than the commonly used TiO_X. The application of a more thermally stable oxide compound used as buffer layer is important, because the postannealing has been shown to yield better device performance,[47,48] because the postannealing is expected to enhance the formation of C−O−Al[8] and Ti−O−Al,[49] improving the interface adhesion, and hence the device PCE.

Figure 4b shows the incident-photon-to-current efficiency (IPCE) spectra of the fabricated devices. Maximum IPCE at 515 nm shows are 65% and 68% for OPV devices with and without TiO_2 buffer layer, respectively. Integration of the IPCE spectra over the visible spectrum corresponds well to the difference in J_{SC} of the devices. The improvement in IPCE with TiO_2 buffer layer is lower than that reported by other group,[31] suggesting the lack of role of our TiO_2 as optical spacer. This supports our hypothesis that the TiO_2 NPs mainly act as ETL/HBL.

In summary, we have improved the performance of P3HT:PCBM based organic photovoltaic devices through incorporation of nanocrystalline TiO_2 buffer layer between the active layer and Al cathode. The TiO_2 NPs were prepared through a simple synthesis from their precursors without any additional hydrolysis process in the air. Maintenance of inert environment during fabrication of devices is important for the use of new materials that may degrade easily in ambient conditions. Because the TiO_2 NPs have better thermal stability than TiO_X, the devices with TiO_2 layer can be subjected to postannealing at elevated temperature. Our results suggest that the TiO_2 buffer layer may only act as the electron transport/hole blocking layer. Under the standard solar cell measurement conditions, PCE of the fabricated devices, 3.94%, was achieved, i.e., ca. 27.5% higher than that of devices without TiO_2 buffer layer. In addition, devices with TiO_2 buffer layer also exhibited better ambient stability as compared to those without TiO_2, as shown in Figure S3 in the Supporting Information. The enhanced stability suggests that the TiO_2 layer could retard the diffusion of

Figure 4. (a) J−V curves obtained under illumination of 1.5G at 100 mW/cm^2 and (b) IPCE spectra of two devices with and without TiO_2 buffer layer.

Table 1. Summary of Device Properties Prepared with and without TiO_2 Buffer Layer

sample	PCE (%)	J_{SC} (mA/cm^2)	V_{OC} (V)	FF	R_s (Ω cm^2)	R_{sh} (Ω cm^2)
without TiO_2	3.09	8.62	0.59	0.60	11.3	464
with TiO_2 (1000 rpm)	3.82	9.64	0.61	0.65	7.7	684
with TiO_2 (2000 rpm)	3.94	10.18	0.61	0.64	6.5	624
with TiO_2 (4000 rpm)	3.86	10.47	0.60	0.62	7.5	717

oxygen/water molecules into the active P3HT:PCBM layer. In the near future, it is important to synthesize more stable and dispersed organic molecule-capped TiO$_2$ NPs. This may help to obtain TiO$_2$ film with more uniform thickness, which in turn is a critical parameter for buffer layer used as optical spacers.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information. TEM images of TiO$_2$ nano-particles, device parameters with/without TiO$_2$ buffer layer, and device parameters as a function of exposure time (PDF). This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Author
*E-mail: hzhang@ntu.edu.sg, ymlam@ntu.edu.sg.

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